

Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claim 1 (currently amended). A flip-flop, comprising:

a clock input for the application of a clock signal;

a data input for the application of a data signal;

a non-inverted output;

an inverted output;

a data acceptance unit having a first switching element and a second switching element;

a storage unit having first and second inverter circuits connected in a feedback loop to provide feedback between said first and second inverter circuits;

an activation input to activate the flip-flop with an activation signal, said first switching element and said second switching element being activated or inhibited, respectively, dependent upon the clock signal, the data signal

Applic. No. 10/699,135
Response Dated March 31, 2005
Responsive to Office Action of January 18, 2005

present at said data input, and the activation signal, causing
information of said storage unit to remain stored
) independently of the clock signal present and the data signal
present, in an event of a deactivated activation signal;

said first inverter circuit having:

a first input; and

a first output coupled to said inverted output;

said second inverter circuit having:

a second input; and

a second output coupled to said non-inverted output; and

said data acceptance unit allocating, dependent upon the data
signal present and the clock signal present, a predetermined
programming potential either to said first input or to said
second input and to apply no potential to the respective other
input of said first and second inverter circuits, said first
switching element of said data acceptance unit applying said
) predetermined programming potential to said first input
dependent upon the clock signal and the data signal, and said

Applic. No. 10/699,135
Response Dated March 31, 2005
Responsive to Office Action of January 18, 2005

second switching element of said data acceptance unit applying
said predetermined programming potential to said second input
) dependent upon the clock signal and the data signal.

Claim 2 (original). The flip-flop according to claim 1,
wherein said first switching element is activated in an event
of a first level of the clock signal and a first level of the
data signal and is inhibited in an event of at least one of a
second level of the clock signal and a second level of the
data signal.

Claim 3 (original). The flip-flop according to claim 2,
wherein said second switching element is activated in the
event of the first level of the clock signal and the second
level of the data signal and is inhibited in the event of at
least one of the second level of the clock signal and the
first level of the data signal.

Claim 4 (original). The flip-flop according to claim 1,
wherein said second switching element is activated in an event
of a first level of the clock signal and a second level of the
data signal and is inhibited in an event of at least one of a
) second level of the clock signal and a first level of the data
signal.

Applic. No. 10/699,135
Response Dated March 31, 2005
Responsive to Office Action of January 18, 2005

Claim 5 (previously presented). The flip-flop according to claim 3, wherein:

said data acceptance unit has a first partially clocked inverter with an output; and

said first switching element is coupled to said output of said first partially clocked inverter to apply an inverted data signal to said first switching element in the event of one of the second level of the clock signal and the first level of the clock signal when the second level of the data signal is present and to apply no potential to said first switching element when the first level of the clock signal and the first level of the data signal are present.

Claim 6 (previously presented). The flip-flop according to claim 1, wherein:

said data acceptance unit has a first partially clocked inverter with an output; and

said first switching element is coupled to said output of said first partially clocked inverter to apply an inverted data signal to said first switching element in the event of one of a second level of the clock signal and a first level of the

Applic. No. 10/699,135
Response Dated March 31, 2005
Responsive to Office Action of January 18, 2005

) clock signal when a second level of the data signal is present and to apply no potential to said first switching element when the first level of the clock signal and a first level of the data signal are present.

Claim 7 (previously presented). The flip-flop according to claim 6, wherein:

said data acceptance unit has a second partially clocked inverter with an output; and

said second switching element is coupled to said output of said second partially clocked inverter and said second partially clocked inverter is connected to said output of said first partially clocked inverter to apply a non-inverted data signal to said second switching element in the event of the second level of the clock signal and to not change the potential at said second switching element in the event of the first level of the clock signal.

Claim 8 (previously presented). The flip-flop according to claim 5, wherein:

) said data acceptance unit has a second partially clocked inverter with an output; and

Applic. No. 10/699,135
Response Dated March 31, 2005
Responsive to Office Action of January 18, 2005

) said second switching element is coupled to said output of said second partially clocked inverter and said second partially clocked inverter is connected to said output of said first partially clocked inverter to apply a non-inverted data signal to said second switching element in the event of the second level of the clock signal and to not change the potential at said second switching element in the event of the first level of the clock signal.

Claim 9 (previously presented). The flip-flop according to claim 7, wherein said first and second partially clocked inverters are configured, in an event of a change in the clock signal from the second level to the first level when the data signal is unchanged, to present the inverted data signal at said output of said first partially clocked inverter and to present the non-inverted data signal at said output of said second partially clocked inverter until the data signal is stored in said storage unit.

) Claim 10 (original). The flip-flop according to claim 8, wherein said first and second partially clocked inverters are configured, in an event of a change in the clock signal from the second level to the first level given an unchanged data signal, to present the inverted data signal at said output of

Applic. No. 10/699,135
Response Dated March 31, 2005
Responsive to Office Action of January 18, 2005

said first partially clocked inverter and to present the non-inverted data signal at said output of said second partially clocked inverter until the data signal is stored in said storage unit.

Claim 11 (canceled).

Claim 12 (currently amended). The flip-flop according to claim ~~[[11]]~~ 1, wherein:

said data acceptance unit has a first partially clocked gate with an output;

said first switching element is coupled to said output of said first partially clocked gate:

to apply an inverted data signal to said first switching element in an event of an activated activation signal and in an event of a second level of the clock signal;

to apply a ground potential to said first switching element in an event of a deactivated activation signal; and

Applic. No. 10/699,135
Response Dated March 31, 2005
Responsive to Office Action of January 18, 2005

in an event of a first level of the clock signal, to
apply either:

the inverted data signal to said first switching
element if a second level of the data signal is
present; or

no potential to said first switching element if a
first level of the data signal is present.

Claim 13 (previously presented). The flip-flop according to
claim 12, wherein:

said data acceptance unit has a second partially clocked gate
with an output;

said second switching element is coupled to said output of
said second partially clocked gate;

said second partially clocked gate is connected to said output
of said first partially clocked gate:

to apply a non-inverted data signal to said second
switching element in an event of an activated activation

Applic. No. 10/699,135
Response Dated March 31, 2005
Responsive to Office Action of January 18, 2005

signal and in an event of a second level of the clock
signal; and

)
to apply a ground potential to said second switching
element at least one of in an event of the first level of
the clock signal and in an event of a deactivated
activation signal.

Claim 14 (previously presented). The flip-flop according to
claim 13, wherein one of said first and said second switching
elements is connected to said first and said second partially
clocked gates to activate, in the event of the deactivated
activation signal and in the event of the first level of the
clock signal, dependent upon the data signal stored in said
storage unit, one of said first and said second switching
element to retain information stored in said storage unit.

)
Claim 15 (previously presented). The flip-flop according to
claim 13, wherein at least one of said first and said second
switching elements is connected to at least one of said first
and said second partially clocked gates to activate, in the
event of the deactivated activation signal and in the event of
the first level of the clock signal, dependent upon the data
signal stored in said storage unit, one of said first and said

Applic. No. 10/699,135
Response Dated March 31, 2005
Responsive to Office Action of January 18, 2005

second switching element to retain information stored in said storage unit.

Claim 16 (currently amended). A flip-flop, comprising:

a clock input for the application of a clock signal;

a data input for the application of a data signal;

a non-inverted output;

an inverted output;

a data acceptance unit having a first switching element and a second switching element;

a storage unit having first and second inverter circuits connected in a feedback loop;

an activation input to activate the flip-flop with an activation signal, said first switching element and said second switching element being activated or inhibited, respectively, dependent upon the clock signal, the data signal present at said data input, and the activation signal, causing information of said storage unit to remain stored

Applic. No. 10/699,135
Response Dated March 31, 2005
Responsive to Office Action of January 18, 2005

independently of the clock signal present and the data signal
present, in an event of a deactivated activation signal;

)
said first inverter circuit having:

a first input; and

a first output coupled to said inverted output;

said second inverter circuit having:

a second input; and

a second output coupled to said non-inverted output; and

said data acceptance unit allocating, dependent upon the data
signal present and the clock signal present, a predetermined
programming potential either to said first input or to said
second input and to apply no potential to the respective other
input of said first and second inverter circuits, said first
switching element respectively applying said predetermined
programming potential to said first input, and said second
switching element respectively applying said predetermined
) programming potential to said second input.